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TEKSCOPE

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TEKSCOPE

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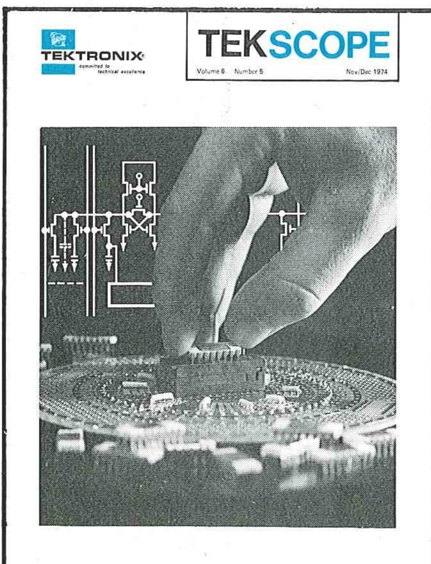
An increasing portion of our time involves working with digital circuitry. A knowledge of the basic logic elements is essential to proficiency in digital servicing. Part I of a two-part article describes the characteristics of one of these basic elements — the flip-flop.

Cover: A close-up view of an activity taking place with increasing frequency — testing of a 4k MOS memory. The lead article in this issue discusses this timely subject.



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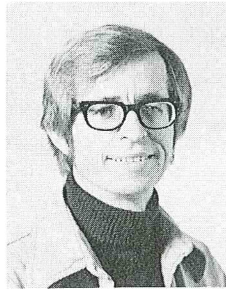
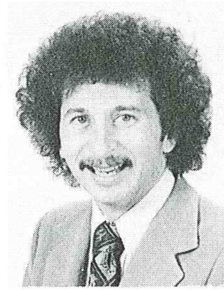
What you need to know about testing 4k MOS memories


William A. Hodge


David H. Flaningam

It's getting so you can't tell a component from a system. Now we have integrated circuit memories in flat packages about an inch long and half an inch wide, able to store 4096 binary bits of information. And the size of the chip in such a package is very small, of course.

But more dramatic than the small size are the low price and the downward price trend. The typical price for these 4-kilobit memories (in large quantities) is between $4 and $8 each. That's 0.1 to 0.2 cents per bit. Regardless of the quantity of 4k MOS memories used to build bigger memories, the price per bit remains essentially constant. With core memories the price per bit decreases when memory size increases. There is a price crossover favoring MOS for the smaller memories and cores for the bigger memories.

The combination of small size and low price is bound to be a winner. The demand for these memories is skyrocketing. For one thing they fill the need for small, inexpensive memories to go with microprocessors, a fast expanding LSI circuit technology itself.

Even though the 4k MOS memory typically has only 22 pins or less, it isn't simple to test. It looks like a small component but resembles a small digital system when you consider what it takes to test one thoroughly. Unlike ferrite core memories the individual components and conductors cannot be tested separately first. And unlike ferrite core memories, failures are not usually catastropic, as a cracked core would be, for example. Sometimes certain combinations of bits won't store, or a bit may not remain stored as long as it should.

The number of possible failure mode combinations is astronomical. Testing all of them is seldom practical because a point of diminishing returns is quickly reached in the test process. An acceptance quality level (AQL) that tolerates up to 1% faulty memories may not be good enough for a user. But a memory manufacturer's AQL that is much better than that may be hard to find, hard to believe, or the product very costly. We should bear in mind, however, that the manufacturer's AQL is based on an extensive set of specifications. Not every user will operate the memory over the full temperature range, nor is he likely to encounter all of the "worst-case" conditions.

It seems clear that part of the money saved in purchasing 4k MOS memories will need to be spent testing them. The question is, how to minimize that expense. Troubleshooting defective electronic equipment at the end of a production line is very costly, and after shipping the equipment the troubleshooting cost is sometimes impossible to calculate. We need to test the device before installing it. Here are a few words about how the 4k MOS memories work and how to test them.

How 4k MOS memories work

MOS memories are built using insulated-gate field effect transistor elements. They have such low leakage that the small stray capacitance associated with each element may be used as a bit storage medium for several milliseconds at a time. The memories are built so that any one of the 4096 storage cells may be examined for a high or

low state, or altered to the opposite state when necessary. This means we have a random access memory (RAM) that we can read or write into at will. It usually takes about 0.5 μs to examine or alter one cell, so it takes about 4000 times as long (2 ms) to examine or alter all cells. Like other semiconductor memories, it completely forgets what was last stored when power is turned off. Furthermore, any cell that has a high level stored in it may discharge to an ambiguous level in a few milliseconds if it is not refreshed. How quickly charge is lost is referred to as memory volatility. That it must be refreshed makes it a dynamic RAM; a static RAM would not have to be refreshed. The leak-down is slow at low temperatures so the maximum refresh period is specified at the maximum allowable operating temperature: for example, 2 ms at 70° C. Figure 1 shows a typical curve of time versus temperature for a type MF7112 memory made by Microsystems International Ltd.

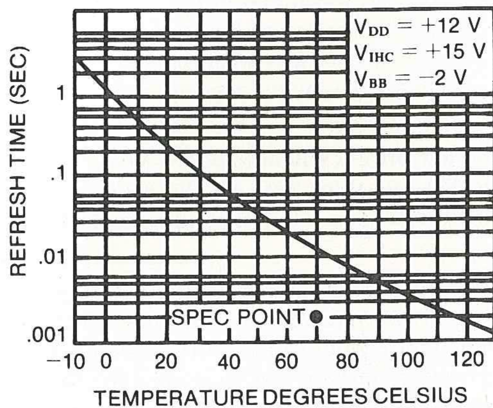


Fig. 1. Shows the effect of temperature on refresh time. Although at 70°C each cell should be refreshed every 2 ms or less, you might be able to wait 10 ms. At 25°C the curve shows refresh time can typically be ten times longer than at 70°C.

Memory configuration

A 4096-bit memory may be arranged with its cells in 64 rows, with 64 cells per row. Or it may have a different configuration, like 32 rows of 128 cells per row. It takes about 0.5 μs to refresh a cell, but an entire row may be refreshed at the same time. The more cells you can refresh at one time, the smaller the percentage of time you need to devote to that part of the business. If you had to refresh only one cell at a time in a 4k memory you would have a full time job just keeping all cells refreshed every 2 ms.

The location of any cell can be identified. First assume that they are all physically arranged in a matrix of rows and columns. The combination of row number and column number may then constitute an address for any cell. To detect the high or low voltage state of a particular cell, or to cause it to go to a particular state, you must first identify the cell by its address. To do that with only 22 pins on the memory, the memory must have two built-in address decoding circuits, a row decoding circuit and a column decoding circuit. A 64 x 64 matrix will usually have six pins on the IC devoted to addressing rows and another six pins devoted to addressing columns. There are 64 possible combinations of high and low states on six lines ($2^6 = 64$) and 4096 possible combinations of high and low states on twelve lines. In other words, each cell would be addressed by a unique combination of states on the twelve address pins on the IC. Some memories have only six address lines and therefore can be built with only 16 pins instead of 22. To address a particular cell with only six lines you must identify the column and row in two sequential steps, with the first half of the address temporarily stored in a latch built onto the memory chip.

For you to write a high or low level into one of the cells, that level must exist on one of the IC input pins reserved for the purpose while the cell is addressed. The line to that pin is usually called Data In. See Figure 2 for a typical set of labels for the different pins on a 4k MOS RAM, a Motorola MCM6605.

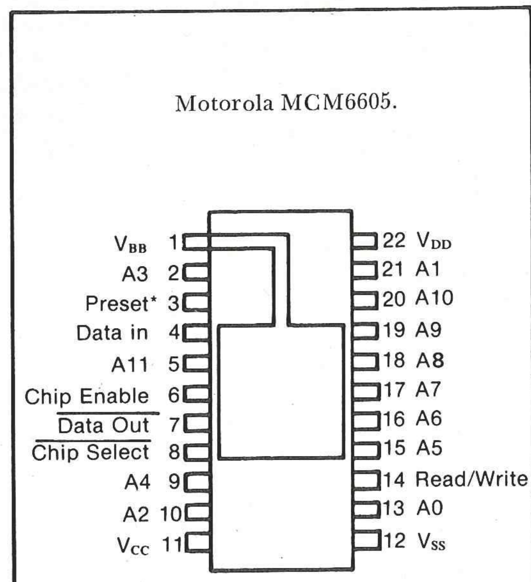


Fig. 2. Shows the pin assignments for a typical 22-pin 4k MOS RAM. The twelve address lines are A0 through A11. V_{BB} is the negative supply voltage, typically −5V. V_{SS} is the reference level voltage, usually 0V (ground). V_{CC} is the positive supply voltage for TTL elements, typically +5V. V_{DD} is the positive supply voltage for MOS elements, typically +12V.

To read the voltage level at a particular cell, the cell is first addressed, then its level sensed and transferred to a pin called Data Output. Whether you write a voltage level into an addressed cell or read a voltage level out of the cell depends on the level you apply to another input pin. That pin is usually called Read/Write or $\overline{\text{Write}}$. One level on that pin makes it possible to read and the other to write. The act of reading should not change the level in a memory; reading is non-destructive. In fact, in some memories, reading a cell also refreshes the cell.

In addition to reading or writing in a MOS memory, an operation called read-modify-write is common. This mode is used when you want to write new data immediately after reading the data already there. The operation makes it unnecessary to wait for a new clock pulse—a big time-saver when you realize how much time you might spend waiting.

Clock pulses mark the moments when the various input

conditions will be examined or the level on the Data Out pin considered valid. The clock line is usually called Chip Enable. On some memories the data output line is able to drive TTL logic circuit directly. In those cases the output line may have three states: High, Low or Floating. Floating is essentially the same as disconnected—unable to influence the circuit it drives.

One or two other inputs are required to make a MOS memory function properly, but precisely what these inputs do and what they are called differs with the type of memory and the manufacturer. In general, however, when these lines are driven with pulses that have the proper timing relationship to pulses driving the other inputs, they make it possible to read, write and refresh in the way intended.

All inputs to some MOS memories may be driven directly by TTL circuits. Other memories may require a drive higher than 5 volts on some inputs. MOS memories that drive TTL circuits directly or accept the drive from TTL circuits usually require a +5-volt supply. A +12-volt supply and a negative supply of −2 volts to −9 volts are also required.

What testers should do

Now let's consider what's involved in testing these memories. In recent years two kinds of tests on digital devices have been identified— functional tests and parametric tests. The merits of the two categories have been debated repeatedly. A simple example of a functional test is what you do when you substitute a new transistor for one you suspect is no good in a circuit that isn't operating properly. If the new transistor restores the circuit to normal operation, it is reasonable to say that the new one functions satisfactorily. Because that's the main thing you want a component to do, some will argue that functional tests which closely simulate the end use of a component are the most important tests a user can make. Others will argue that simulation is seldom perfect, and that the only justification for calling a component defective is that it does not do what the manufacturer claims it will do. When a component is tested to determine whether a particular characteristic (parameter) meets the claims of the manufacturer, the test may be said to be a parametric test. Parametric tests may be categorized as dc tests or ac tests, depending on whether the characteristic being tested applies to a steady state (dc) condition or a dynamic (ac) condition. Both parametric and functional testing are usually advisable for users of complex components like 4k MOS memories.

Testing a memory to see whether it will work satisfactorily in your equipment includes being sure every cell can store both a high level and a low level. There are several ways to test for this. You might write a high into each cell, then check that you read a high from each cell. After that you would write a low into each cell and check that every cell read low. The cells can be addressed in any sequence when writing or reading. Another way of making this test is to alternate between writing a level and reading that level, progressing from cell to cell. To read and write both a high and a low state on every cell takes 16,384 operations (4 x 4096).

Other similar tests that take more operations, and consequently more time, should follow this test. If a given memory did not pass this fundamental test, however, further testing might be pointless. It is desirable to have the testing equipment able to discontinue a test and reject a part at any time. It is also desirable to segregate defective memories according to the fault that is the basis for rejection. Suppliers who accept them for credit want to know why you consider them defective.

Test patterns

Some MOS memory cells may write and store properly under all conditions except one following a particular sequence of memory operations. For example, because MOS memory cells rely on stray capacitance as a storage medium, the charge status of a cell can sometimes be altered when an adjacent cell switches states. To exercise a memory in a way that tests this possibility requires a particular test pattern. Some patterns for testing 1024-bit memories have become fairly common and are given names like Walk Data, March, Ping-pong. The Ping-pong pattern addresses successive memory cells in all possible combinations and takes about 2 seconds (over 4 million operations) to exercise a 1k MOS memory. To test a 4k MOS memory using the same pattern would take about 32 seconds, 16 times as long. Such patterns require an amount of time proportional to the square of the number of cells and are, therefore, called N^2 patterns.

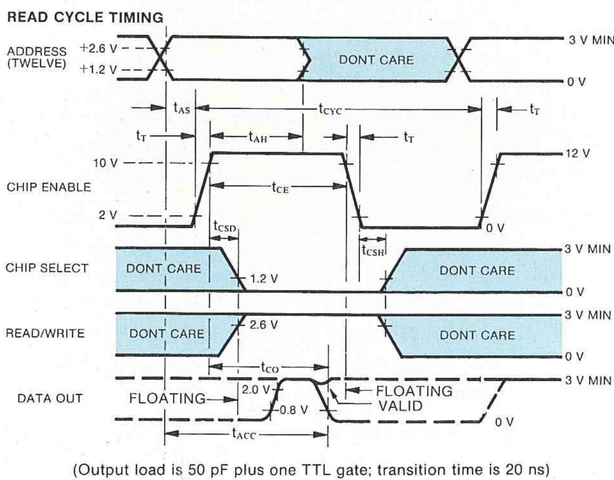
Incidentally, N^2 test patterns don't always exercise even 1k MOS memories the way you think. In some memories a particular cell (the one with the highest address number) is addressed by the mere act of disabling the address inputs to any other cell. That, in effect, makes each new address follow the same old address, limiting the number of combinations to N instead of N^2.

Thirty-two seconds for a single test may be prohibitive from an economic standpoint. Different test patterns have been developed to test 4k MOS memories so they may be tested in shorter, more reasonable periods of time with comparable certainty of detecting faults. New and better test patterns will be developed. Some patterns work better on one type of 4k memory than another because of differences in construction. A knowledge of the layout (topology) of the thousands of microscopic parts of a memory helps. It is also helpful to be familiar with the most likely causes of failures. The test program can then be written to disclose the greatest number of faults in a minimum of test time.

Technical requirements

There are a few important technical requirements a MOS memory tester should meet. Some of these requirements may be more fully appreciated by taking a look at the read-cycle timing waveforms that are a part of a typical 4k MOS memory spec sheet, Figure 3. All but the last of these pulses must be generated by the test equipment and delivered to the device input pins, free from overshoot and ringing, with accurate amplitude excursions and transition time (slew rate). There are also some critical timing relationships between input pulses that must be observed. For example, the leading edge of the Chip Enable pulse must not occur ahead of the leading edge of any of the twelve address pulses. It

is not easy to generate and deliver fifteen pulses so that they arrive simultaneously. The tester must be able to receive and examine the state of the Data Out pulses, as well as deliver properly timed input pulses in a programmed test pattern. To test the validity of any output pulse, the tester must know beforehand what the proper state of the output pulse is, and be able to test for it at precisely the right moment. Knowing the input conditions lets you predict what the output pulse state should be for any test cycle, so the actual output is compared with the predicted output. The moment of comparison (strobe timing) is critical because in most MOS memories the output pulses don't remain in a high or low state long in each cycle but quickly change to a floating state. It is also critical because of the transmission delay time introduced by the cable that connects the test system to the memory test fixture. Delay time is constant, however, and a well-designed tester takes this into account.



(Output load is 50 pF plus one TTL gate; transition time is 20 ns)

CONDITION (C) OR CHARACTERISTIC (*)			MIN	MAX
t_{AS}	Address Set-up Time	(C)	0	—
t_{CYC}	Read Cycle Time	(*)	470 ns	—
t_{AH}	Address Hold Time	(C)	60 ns	—
t_T	Transition Time	(C)	—	100 ns
t_{CE}	Chip Enable Time	(*)	310 ns	—
t_{CSD}	Chip Select Delay Time	(C)	0	70 ns
t_{CSH}	Chip Select Hold Time	(C)	0	—
t_{CO}	Chip Enable-To-Output Time	(*)	—	280 ns
t_{ACC}	Read Access Time	(*)	—	300 ns

Fig. 3. Shows input and output waveforms, their timing relationships, and timing requirements for a read cycle.

Comparison of the state of an actual output pulse with the state of the predicted output pulse is done in a digital comparator. When the states are not alike, an error is detected and the component judged defective. To make sure that comparisons only occur when they should, the comparators are strobed. Strobe pulses are generated by the tester at moments when valid memory output data should be arriving back in the comparator. Those moments begin in each cycle when the specified maximum access time has expired, and they end at some specific later time depending on whether the cycle is a read or write cycle. A tester should be able to generate fast, clean comparator strobes that begin and end with precise timing.

Digital comparators basically tell whether two levels are the same or not the same: that is, both high or both low, or one high and the other low. But there are limits to what may be called a high level and what may be called a low level. The better digital comparators check highs and lows against different reference levels. These comparators are called dual-level comparators. The high and low reference levels should be programmable, in small, accurate increments over an adequate range, to correspond with the memory manufacturer's definitions of high and low limits. With dual-level comparators you can test for the effects of noise voltage spikes on output data. For example, noise spikes big enough to alter a +2.4 volt high level to a +1.7 volt level would go undetected if +1.5 volts were selected as both the lower limit of a high level and the upper limit of a low level. See Figure 4.

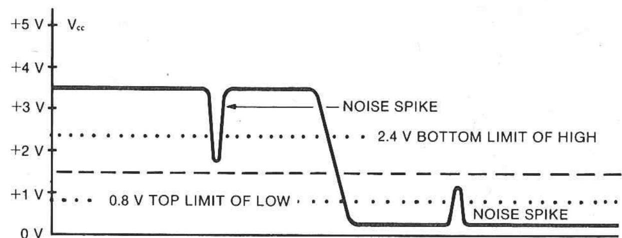


Fig. 4. Noise spikes would not be detected by single-level comparator set for +1.5 volts but would be detected by dual-level comparator set for +2.4 V and +0.8 V.

Other considerations

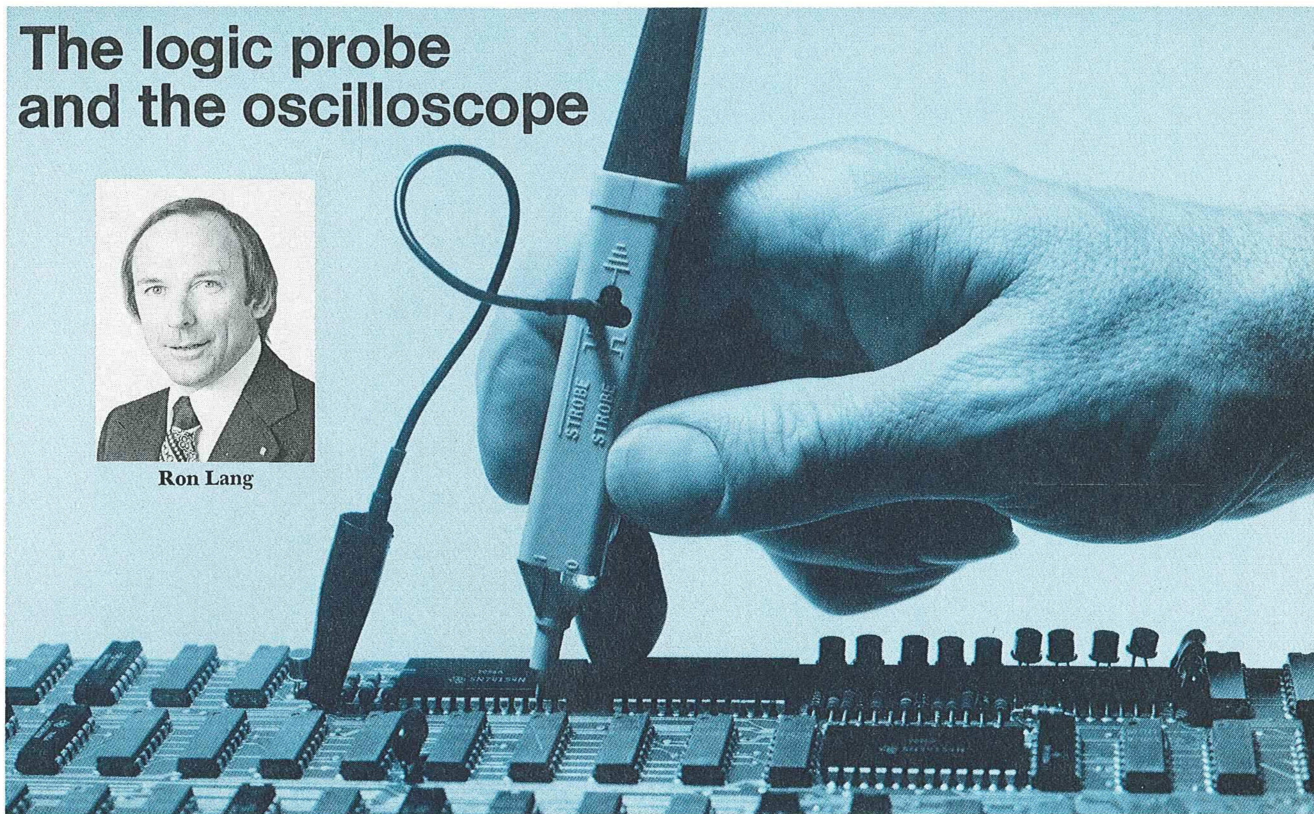
There are other important factors to know about when considering what a memory tester should do. Because testers must be automated to conduct all the necessary tests in a short period of time, they are not inexpensive. You should consider how many other jobs they may do when you look at the price. You should also consider obsolescence and expandability. Data bus construction helps assure versatility and expandability, and insures against obsolescence, Data bus construction merely means that all the controllable modules, sections, and pieces of equipment get instructions from the system controller section on common data lines. To add a piece of equipment means that you connect it in parallel to the other pieces on the same lines (data bus), and that it ignores all data until it is addressed by the system controller.

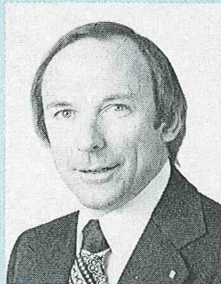
You spend a good part of the time required for testing devices like MOS memories in handling the devices—inserting them into and removing them from the test fixture. To avoid wasting time, two test fixtures may be used with one test system. One fixture is involved with the removing and inserting process while the other conducts tests. A system

which can switch its tests automatically in this way should pay for itself much more quickly than one that can't. These considerations are only samples. There are numerous others.

We believe 4k MOS memories will have a dramatic influence on the design of new electronic equipment. We also think most engineers, technicians and managers will need at least a good conversational knowledge of how MOS memories work and some of the basic problems in testing them. However, you may need to know more than most people about testing these memories, and probably much more than has appeared here. In that case, our Application Engineers would be glad to talk to you. They will want to tell you all about the TEKTRONIX S-3400 series of test systems that we believe do an outstanding job of testing MOS memories and similar devices. You'll find them good listeners, too.

The logic probe and the oscilloscope





Ron Lang

When the logic probe first appeared on the measurement horizon, it was touted by some as a low-cost replacement for the oscilloscope in troubleshooting and servicing digital logic circuitry. Time has, indeed, proven the logic probe to be a valuable tool in working with digital logic: not as a replacement for the oscilloscope but rather as a valuable adjunct.

The province of the logic probe is fast failure detection, that of the oscilloscope in-depth analysis — a perfect complement. With the logic probe the user can often quickly locate a circuit fault or failure. The oscilloscope is then brought into play to analyze the character of the fault or failure.

Although designed primarily for fast checking and troubleshooting of existing digital circuits on location by service personnel, the logic probe is also a time-saver for designers of circuits being breadboarded.

A digital logic probe's sole function is to indicate the state of the logic: high, low, or faulty, i.e., open or in the indeterminate range. There are many logic probes that do this. They use incandescent lamps or light emitting diodes as indicators. Some probes have a one-light readout using a bright and a dim indication; others have two, three, or four light systems; and at least one uses four LEDs as the readout.

There is also a variety of options to choose from. In some cases, these options are attached to the probe externally. Included are storage or memory, fast response or slow response, strobe input, and accessory packages.

The TEKTRONIX P6401 TTL Logic Probe combines all the features needed to verify any logic condition in one small, lightweight package. Two lights, red and green, are located in the nose of the probe. There they can be easily viewed without moving your eye from the point under test. The red light indicates logic 1 (2.15 to 5 V dc) and the green light logic 0 (0 to 0.7 V dc) in the following manner:

Logic State	Indication
Steady high state	Steady red light
Steady low state	Steady green light
Pulse trains (normal switching)	Blinking red and green lights at full intensity
Abnormal state (between high & low)	No lights
Open circuit (greater than 10 kΩ)	No lights
Excessive input voltage (greater than 6 volts)	Both red & green lights lit
Alternating between high state and indeterminate state	Blinking red light
Alternating between low state and indeterminate state	Blinking green light
Single pulse (+)	Green, red, then green
Single pulse (–)	Red, green, then red.

The P6401 has a fast response time and recognizes pulse widths as short as 10 ns. The circuitry controlling the indica-

tor lights has a built-in stretch feature. Once a light is turned on, the circuitry holds it on for 100 ms; once extinguished, it won't allow it to turn on again for 100 ms. In the observation of rapid pulse trains, this gives time to turn the light on and time to let the eye recognize that the light has come on and turned off. If the signal repetition rate is below 5 Hz, the blinking of the lights will follow the signal repetition rate. When the point being observed exceeds about 6 V dc, both red and green lights will glow steadily. This lets the operator know that an over-voltage condition exists in the circuitry being checked. Built-in protection for the probe input permits momentary overloads up to ±150 V dc or rms without damage to the probe. At high-input voltages, an easily resettable fuse in the input will open and prevent circuit damage. Probe input impedance is high in all states (7.5 kΩ paralleled by 6 pf) so as not to disturb the circuit under test.

The length of ground path returns is an often overlooked consideration in the use of logic probes. The P6401 has provision for plugging a short ground lead directly into the probe. This is the same ground as the negative, or black, power lead, but provides a considerably shorter path for the fast-signal acquisition encountered in TTL circuitry. This eliminates ringing and overshoot that could cause false light indications. Short ground leads should be used in all measurements.

Many features that are optional or even add-on modules on other logic probes are standard on the P6401 — for example, the "store" mode. This holds the light readout on until manually reset and is a valuable aid in single-pulse detection. As mentioned previously, pulse widths as short as 10 ns can be detected and indicated by the readout lights. Another feature, the "strobe" or gate mode, is employed when the coincidence of logic levels at two points needs to be confirmed.

The P6401 at work

Let's put the P6401 to work in actual circuits and see how it performs. Power is usually applied to the probe from the circuit under test through convenient clip leads attached to the probe. The red lead attaches to the +5 V dc bus and the black lead to the ground reference bus. Now simply touching the probe tip to the point under investigation will indicate the logic condition.

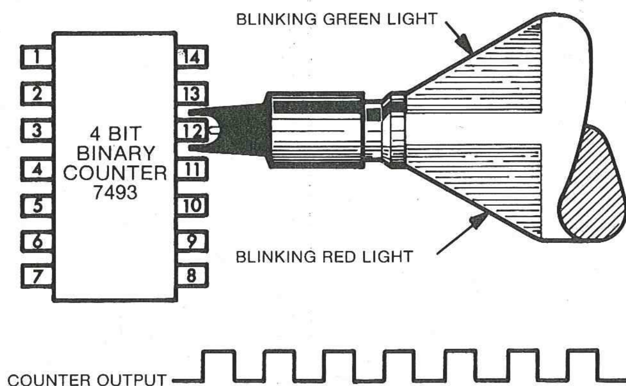


Fig. 1. P6401 measuring the output of a binary counter. The IC-lead adapter on the probe nose prevents slipping off the pin and causing circuit damage.

In Figure 1 the logic probe is being used to check the output of a binary counter. The red and green lights will blink on and off at a 5-Hz rate indicating that the logic level is transiting from logic 0 to logic 1 and back.

The IC Test Lead Adapter used in this application was designed especially for IC chip leads. It prevents the probe tip from slipping from the lead under test and causing faulty indications or disrupting circuit operation. It is also convenient for probing components mounted on circuit boards, such as resistors, capacitors and diodes.

Figure 2 shows the logic probe being used to verify the inputs and outputs of a positive NAND gate. When the two inputs are low, the output is high; when pin 8 is probed, the red light will come on. If the inputs, pins 9 and 10, are probed the green light will come on, indicating a low state.

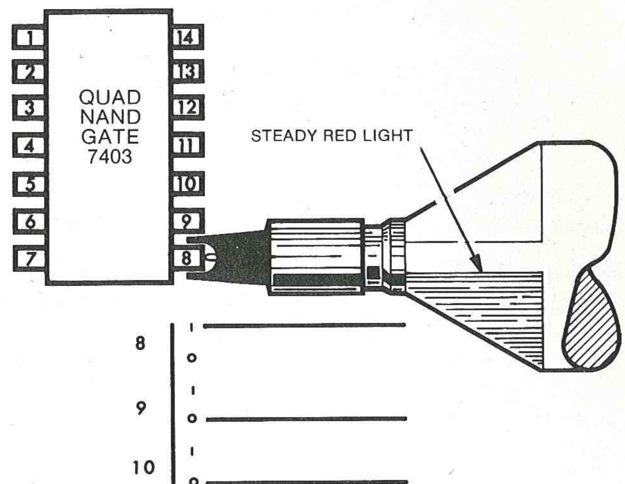


Fig. 2. The P6401 indicating the output of a NAND gate.

Often it is necessary to know if an event has happened. This may be a pulse that happens only once in several minutes. Here the "store" feature of the probe is used to capture a single pulse that may be as narrow as 10 ns. Switch the logic probe to the "store" mode with the switch located on the probe. It can now be attached to the test point to be monitored. (See Figure 3.) The green light comes on and stays on when pin 8 is probed; this is a logic 0. The red light turns on when the four inputs become positive, causing the output, pin 8, to go positive, a logic 1 state. The two lights will stay on even if the probe is removed from pin 8. To reset the probe, slide the "store" switch back. If the "store" mode is needed again, simply push the "store" switch forward. If desired, the probe may be attached to the circuitry and left unattended. When the event happens, the appropriate light will come on and remain on indefinitely for a record of the event.

Many times it is desired to detect the coincidence of two pulses. The P6401 has this capability as a standard function. To determine coincidence, the strobe input of the probe is connected to the strobe point that the event is to coincide with, such as a gate or strobe pulse. If the gate or strobe is a negative pulse, connect the strobe lead to the $\overline{\text{strobe}}$ (strobe not) input on the probe. With the probe tip, monitor the

point in question. (See Figure 4.) If the indication of the event is to be retained, the "store" mode may be used in combination with the strobe.

The probe recognition circuitry is gated off until the advent of the strobe pulse. Therefore, whatever transitions occur at the probe tip will not turn on a light. When the strobe does occur, the probe is gated on. An event at the probe tip will be indicated by the lights and retained if the "store" mode is used. If the event does not happen for at

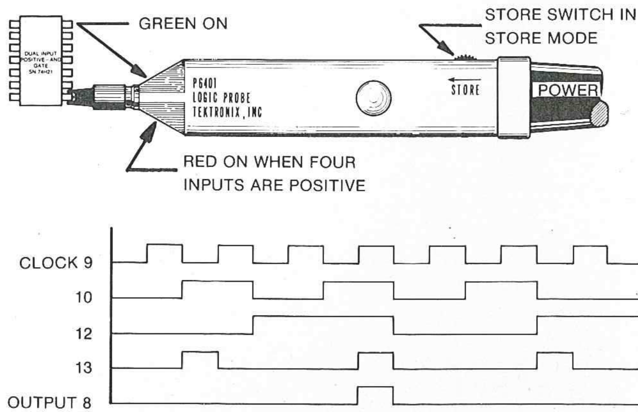


Fig. 3. The P6401 used in the "store" mode to indicate coincidence of four events. Pulses as narrow as 10 ns can be captured in the "store" mode.

least 2 ns after the strobe, the green light will come on first, and stay on if in "store" mode; then the red light will come on and stay on. Because of the short, 2-ns, period both green and red lights will appear to come on together.

If, as in the techniques shown, the desired event does not materialize, the problem can be traced to a faulty component such as an IC chip having the appropriate inputs but a wrong output. The faulty component can then be replaced and the circuit put back into correct operation, or an oscilloscope can be used to examine exact wave shapes and voltage levels for an in-depth analysis of the problem.

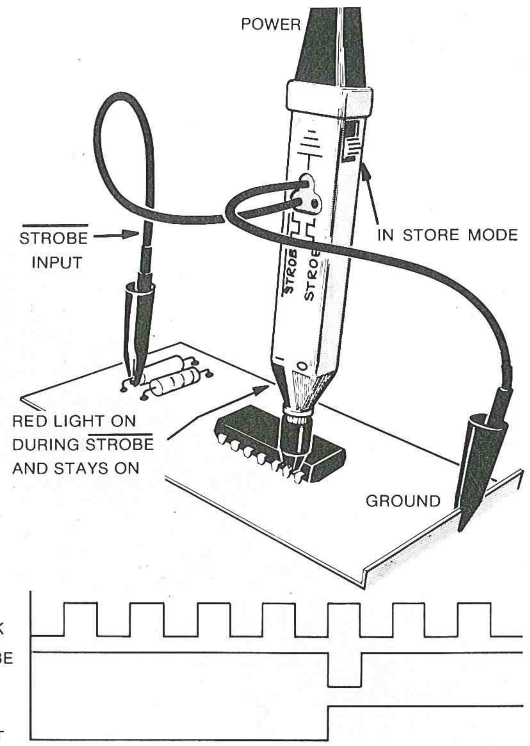


Fig. 4. The STROBE function is used to determine if an event occurs during a strobe, or gate, interval.

In summary, the P6401 Logic Probe is a lightweight, dynamic, decision-making tool that derives its power from the circuit under test to determine logic states. It can quickly find faults that can be corrected on the spot. Used alone or with an oscilloscope the logic probe is finding increasing use in designing and troubleshooting systems such as point-of-sale terminals, computers, inventory control systems, video tape record and playback systems, readout systems, or any other system using TTL logic, singularly, or in combination with any other logic family.

Teknique

Understanding oscilloscope triggering controls

Modern oscilloscopes offer a wide choice of triggering controls that enable us to trigger on almost any signal. One recently introduced portable oscilloscope has twenty controls on the front panel. The popular TEKTRONIX 465 and 475 portables each have twelve — more than you would expect. Why so many triggering controls and what do they all do?

The modern oscilloscope is a versatile, general purpose instrument used in many disciplines. We want to display and measure a wide variety of signals and we need to "stop" them to do so. That means we have to be able to trigger on them. There are also many applications, such as photographing single-shot transients, that call for special triggering controls. You may never need to use them in your work, but many people do, so you find these controls on most scopes.

Another factor contributing to the large number of triggering controls is that many scopes have two sweeps — a delaying and a delayed, each with its own set of triggering controls.

Now let's look at each control: what does it do and when should it be used? Triggering controls can be divided into four groups: triggering source, coupling, mode, and variable controls such as trigger level and holdoff.

Trigger source

As the name implies, the trigger-source controls determine the origin of the signal that will be used for triggering. There are usually three sources:

1. Internal — part of the signal fed into the vertical amplifier, and the source most commonly used. In multichannel or dual-beam scopes you also need to choose which channel, or beam, you will trigger from internally. This choice is often a source of triggering problems. What typically happens is we feed the vertical signal into one channel and fail to notice that the trigger selector is set to the opposite channel. Another pitfall is trying to operate in the ALTernate mode with only one input signal.
2. External — from a source external to the scope. This signal is fed into the external trigger input connector. The most common problem here is that the signal amplitude often exceeds the range of the trigger level control. Some scopes have an EXT ÷ 10 position to attenuate the external signal. An alternate solution is to use a probe on the external input. Use of a probe has the added advantage of minimizing loading on the trigger source.

   External triggering is convenient when you're viewing a series of events keyed to a single pulse, such as the index pulse on a disc memory, or to a stable source like the clock pulse used in digital circuits. It also allows for the use of an external device, such as the TEKTRONIX 821 Word Recognizer, to generate a single trigger pulse from a selected pattern of pulses such as a digital word.
3. Line — derived from a low-voltage winding on the scope power transformer. The line source is especially useful when viewing small ripple voltages on power supplies. It is also useful for viewing the fields in a television signal and other events related to the power line frequency.

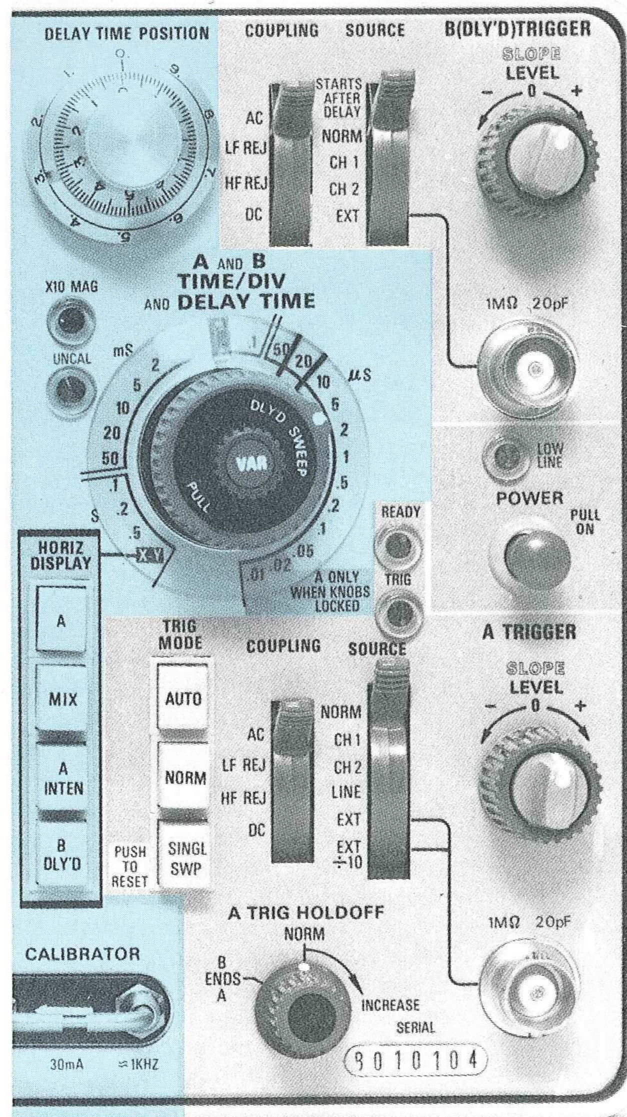


Fig. 1. Triggering controls on the 475 are kept at a minimum by using multi-position switches for trigger source and coupling. The SINGLE SWP pushbutton also serves as the RESET control for single-shot sweeps.

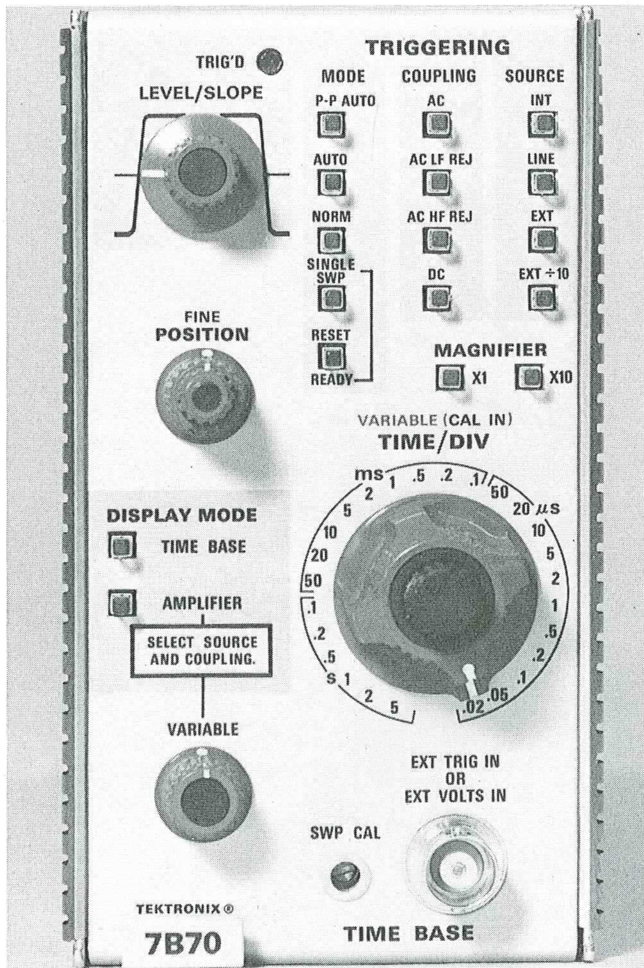


Fig. 2. The 7B70 Time Base uses separate pushbuttons for selecting triggering mode, source and coupling. Hands-off triggering is accomplished by actuating the three uppermost pushbuttons. Trigger level and slope.

Trigger coupling

The trigger coupling controls are, basically, passive filters that eliminate unwanted signals. Choices of coupling usually include dc, ac, ac low-frequency reject, and ac high-frequency reject. The frequency range of the various coupling positions on the TEKTRONIX 475 are shown in Figure 3.

Dc coupling is used to trigger on slowly changing signals such as a slow ramp, on low-repetition-rate signals, or to trigger at a given dc level. On most scopes, when you use internal triggering, you can set the trigger level control for triggering at a dc level represented by some point on the crt screen. You can easily verify the setting by rotating the vertical position control and noting that triggering takes place at the desired point. On other instruments the trigger takeoff is ahead of the vertical position control, and you can't predetermine the dc trigger level setting without using an external signal. This configuration has the advantage that the vertical position control has no effect on the dc triggering point.

The ac coupling positions avoid the effects of dc present in the triggering signal. In the AC position, signals from about 60 Hz to the upper bandwidth limit of the vertical amplifier are passed to the trigger circuits. In some instances, undesirable frequencies riding on the triggering signal cause problems. Low-level signals often contain hum induced by stray magnetic fields. You can get rid of the hum by using AC LF REJECT coupling. Conversely, you can eliminate high-frequency noise causing triggering problems, by using AC HF REJECT coupling. You will, no doubt, use the AC coupling position most often, but you will also find the other positions valuable in difficult triggering situations.

Trigger modes

There are at least three triggering modes available on modern oscilloscopes: automatic, normal and single-sweep. Peak-to-peak automatic, a special form of automatic, is included on some instruments. High-frequency sync is usually found on wide bandwidth and sampling instruments.

In the automatic, or AUTO, mode the sweep free-runs in the absence of an adequate trigger signal. This provides a convenient reference trace on-screen. Early scopes with AUTO triggering had no trigger level control in the AUTO mode. The signal being viewed was superimposed on a regenerative trigger signal generated in the trigger circuitry. When the combined signal reached the appropriate level the sweep was triggered. This permitted you to look at different amplitude signals in a circuit without having to readjust the trigger level control. With the AUTO mode in today's instruments, trigger level control is maintained. When the signal is outside the range of the level setting, the sweep free-runs. This type of free-running display is useful when measuring the peak-to-peak amplitude of a signal without observing the waveshape, as in bandwidth measurements.

In the P-P AUTO mode the peak-to-peak amplitude of the trigger signal is impressed across the trigger level control. If you have an adequate trigger, the sweep will be triggered regardless of the level control setting. So you can look at different signal levels without adjusting the level control, but you maintain control of the point at which triggering occurs.

The NORMAL mode is so called because it handles the widest range of triggering signals. It is the mode normally used when you have a complex waveform to trigger on, or when the signal frequency is outside the range handled by the AUTO mode. In the NORMAL mode, the sweep will not run in the absence of a trigger, so you have no reference trace.

HF SYNC is typically used when the amplitude of the high-frequency signal is too low to trigger on solidly, or when the frequency is beyond the bandwidth capabilities of the trigger circuit. The TRIGGER LEVEL and TRIGGER HOLDOFF controls usually serve as the sync control in this mode.

The SINGLE SWEEP mode is used when you want to photograph transients or low-repetition rate events. Here's the usual procedure. Set up the triggering controls in the NORMAL mode, using the calibrator as a signal source to simulate the transient. Then, with the calibrator signal still applied, go to the SINGLE SWEEP mode and adjust the intensity and focus controls while pressing the RESET button repeatedly. Once the setup is completed, remove the

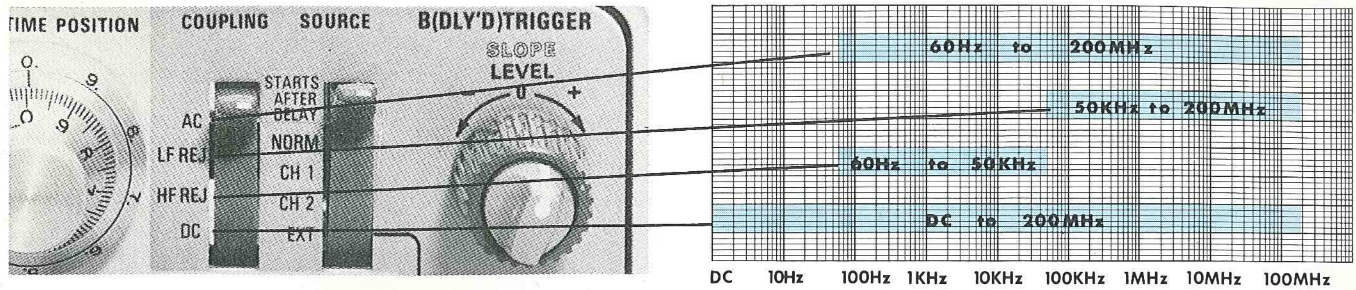


Fig. 3. Frequency range of each position of the COUPLING switch.

calibrator signal and apply the signal input lead, open the camera shutter, and press the RESET button. The READY light will come on, indicating that the sweep is ready to receive a trigger. When the event occurs and the sweep is triggered, the READY light goes out, indicating that a sweep has occurred. The camera shutter is then closed. Clearly, this procedure is much easier than trying to synchronize the camera shutter to the event.

Trigger level, slope and holdoff

Trigger level and slope selection are sometimes combined in one control, as in Figure 4. More often they are separate controls. Trigger slope refers to the direction the leading or trailing edge of the signal traverses when triggering takes place. It does not refer to the dc level of the signal. For example, if the SLOPE control is in the plus (+) position, triggering will occur on the rising portion of the waveform. In the minus (–) position, triggering will take place on the falling portion.

The TRIGGER LEVEL control selects the point on the slope where triggering will occur. When triggering internally you should be able to trigger at any point on an on-screen display. If you have a display several divisions in amplitude, the TRIGGER LEVEL control will have a wide range over which the sweep can be triggered. For low-amplitude displays triggering will occur near the 0 setting of the LEVEL control and triggering will seem to be very touchy. That's because

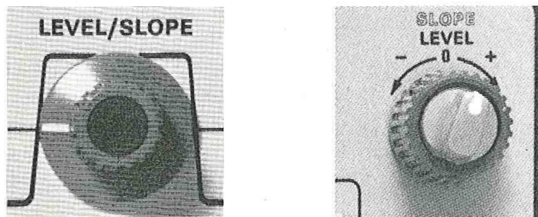


Fig. 4. Two methods of handling the TRIGGER LEVEL and SLOPE function. Both functions are accomplished with one control shown at left. Concentric controls at right accomplish both functions and occupy about the same front-panel space.

the LEVEL control doesn't have much signal over which to range. The range of the TRIGGER LEVEL control when triggering externally is different for different instrument types. It will typically be at least +1.5 V to –1.5 V in the straight-through position and +15 V to –15 V in the EXT ÷ 10 position.

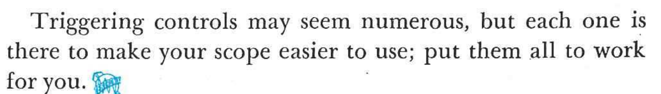
The TRIGGER LEVEL control cannot discriminate between pulses of the same amplitude. This is where the TRIGGER HOLDOFF control comes into play. You may want to trigger on a particular pulse in a pulse train, but the pulses normally have the same amplitude. When the sweep recovers and is ready to be triggered, the next pulse will trigger it. Depending on the TIME/DIV setting and the sweep recovery time, triggering may or may not occur at the same point in the pulse train each time, and the display will be unstable. The holdoff control lets you adjust holdoff time to avoid this condition. If your scope doesn't have a holdoff control, you can achieve the same effect using the VARIABLE TIME/CM, but the sweep will be uncalibrated. If the scope has a delaying sweep, SWEEP LENGTH can serve as a holdoff control.

Summary

Oscilloscopes typically have many triggering controls. But each serves a useful purpose. For most of your work, you probably need only a few trigger controls. But when you run into a less-than-ideal triggering signal, you will find those "extra" controls indispensable.

On Tektronix instruments we make it as easy as possible to use the triggering controls. For example, with all of the trigger switches in the "up" position, or the top row of trigger pushbuttons depressed, you should have a trace on screen. If the display is not stable, a slight adjustment of the TRIGGER LEVEL control may be all that is necessary. In most cases it's that simple.

Triggering controls may seem numerous, but each one is there to make your scope easier to use; put them all to work for you.



Servicescope

Troubleshooting digital circuits

If you haven't had much cockpit time troubleshooting digital circuits, you probably think it's a tougher job than it is. Most every experienced troubleshooter you talk to who knows both analog and digital circuits agrees that digital circuits are much easier to troubleshoot.

Just as the analog man needs to know about transistors, gain, feedback, dividers, etc., the digital man needs to know about AND gates, OR gates, inverters, flip-flops, and multivibrators. The vast majority of digital integrated circuits are made up of these elements or combinations of them. Of the group, flip-flops and multi-vibrators are probably the toughest to learn and retain. Therefore, Part I of this discussion will review flip-flop fundamentals.

PART I Fundamentals of flip-flops

Most flip-flops have two outputs, designated Q and $\overline{Q}$, or sometimes 1 and 0. The two outputs are complements of one another; if Q is at a high level $\overline{Q}$ will be at a low level and vice-versa. Sometimes only one of two outputs is used and in that case the unused output line may not even be drawn on your schematic. Don't let that confuse you. The distinguishing symbols are the input symbols. All lines except Q and $\overline{Q}$ are input lines.

T flip-flops

The simplest flip-flop is the T flip-flop, sometimes called the triggered flip-flop. It has only one input; others have at least two. The purpose of the T type flip-flop is to provide an output which switches to its opposite state each time a trigger pulse is introduced. When the outputs reverse from a given state the IC is said to toggle. A T type flip-flop can be made by connecting together several inputs on the J-K flip-flop.

D flip-flops.

Next in simplicity is the gated D type flip-flop, sometimes called a latch. This type of flip-flop allows binary data to be transferred from the D input to the Q output when the gate input (G) is at the proper level but blocks the transfer of data when the G input is in the opposite (unasserted) state. When the G input goes to the unasserted state the outputs remain (latch) in their existing states.

Clocked D type flip-flops only transfer data when a clock pulse arrives. The level at D is then transferred to the Q output and the level at Q remains until the next clock pulse arrives. If the data input level is the same as when the last clock pulse arrived there will be no change in output. You could say the output is updated just the same. The symbol for the clock input is usually CK, with the input marked with an arrow point (⊸▷). CP, CL or C are also used and the arrow point is sometimes omitted.

Clocked R-S and J-K flip-flops

Practically all R-S flip-flops and J-K flip-flops are clocked. The J-K inputs on a J-K flip-flop are the data input lines. The R-S inputs on an R-S flip-flop are the data input lines. The state of the outputs on an R-S or J-K flip-flop depends on the combination of states of the two data input lines when a clock pulse arrives. For an R-S flip-flop there are four combinations: (1) S HIGH and R LOW, (2) S LOW and R HIGH, (3) both LOW, and (4) both HIGH. For a J-K flip-flop the same combinations of J and K inputs apply.

There is no difference in behavior between an R-S and a J-K flip-flop except for the combination where both data inputs are HIGH. For R-S flip-flops the output levels of both the Q and $\overline{Q}$ lines are indeterminate when both data inputs are HIGH when clocked. For J-K flip-flops both output levels switch (toggle) from their existing states if both J and K are HIGH when clocked. The outputs of R-S and J-K flip-flops do not change if both data inputs are LOW when clocked.

If the two data inputs are in opposite states when clocked, the Q output should go to the same state as the S input of the R-S flip-flop, and to the same state as the J input of the J-K flip-flop. Schematically the output lines are normally drawn directly opposite the inputs to which they correspond. That is, Q is drawn opposite the S input on R-S flip-flops and opposite the J input on the J-K flip-flop, while the $\overline{Q}$ output is drawn opposite the R input or K input.

Edge-triggering and pulse-triggering (Master-Slave)

Clocked flip-flops are said to be edge-triggered or pulse-triggered. When pulse-triggered the outputs should not change until the trailing edge of the clock pulse occurs. When edge-triggered, no reference is made to the leading or trailing edge of the clock pulse. Input data is transferred to the output during and immediately following the activating transition of the clock pulse. An activating transition may be up-going or down-going, but not both, depending on the flip-flop.

Both up-going and down-going transitions of the clock pulse activate something in master-slave flip-flops. One edge stores the levels of the data inputs in the flip-flops and the other edge transfers the stored data to the output lines. Each output transfer has to be preceded by input storage, so you can say the leading edge stores and the trailing edge transfers. This must be kept in mind when a master-slave flip-flop is checked for proper operation because input data sometimes switches in the interval between the leading and trailing edges of the clock pulse. That is not usually the case but when diagnosing a trouble it may be particularly confusing.

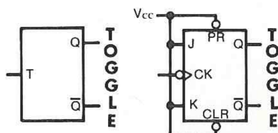
Complicating diagnosis even further is the fact that some master-slave flip-flops will always store the high level if the data input level changes between leading and trailing edges. This happens whether the high level occurs first or last and is called "ones catching". Master-slave flip-flops with "data-lockout" store only the level seen during and immediately following the leading edge transition.

The accompanying diagrams for the various flip-flops should help clarify their operation for you.

In the next issue of Tekscope we will discuss some basic techniques for troubleshooting digital circuitry.

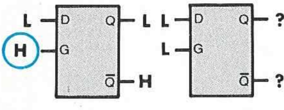
T Type Flip-flops

Each input pulse causes the outputs to reverse.



Gated D Type Flip-flops

The Q output follows the data (D) input when and only when enabled by the gate (G) input.



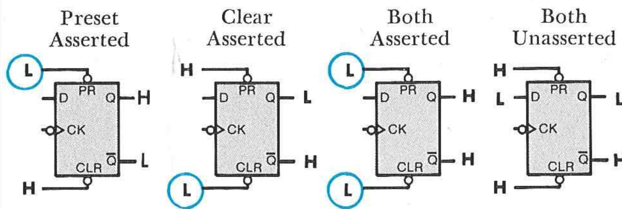
Clocked D Type Flip-flops with Preset and Clear

Asserting Preset or Clear overrides all other inputs.

Asserting both produces two HIGHS at the output, but both HIGHS will not persist even if Preset and Clear are unasserted at the same time.

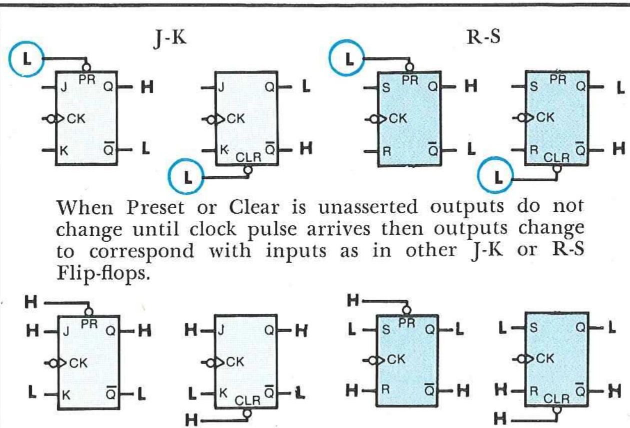
When both Preset and Clear are unasserted clock pulses transfer the D input state to the Q output.

Preset Asserted	Clear Asserted	Both Asserted	Both Unasserted



J-K and R-S Flip-flops with Preset or Clear

Asserting Preset or Clear overrides all other inputs.

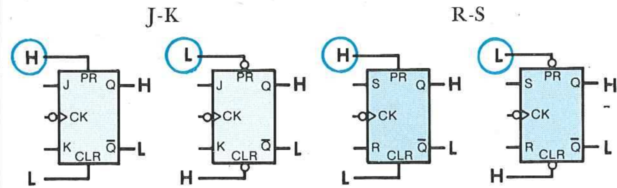


When Preset or Clear is unasserted outputs do not change until clock pulse arrives then outputs change to correspond with inputs as in other J-K or R-S Flip-flops.

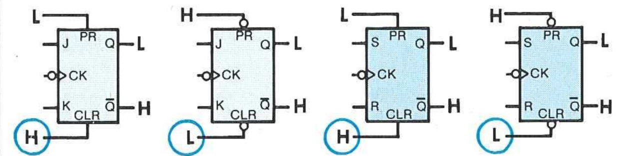
J-K and R-S Flip-flops with Preset and Clear

Asserting Preset or Clear overrides all other inputs.

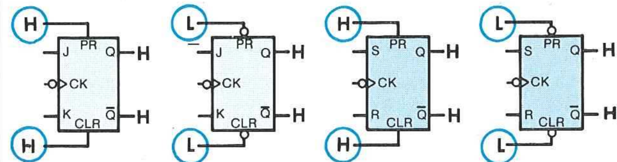
When Preset is asserted (but Clear is not) Q goes HIGH and all other inputs are irrelevant.



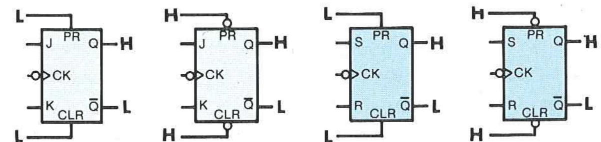
When Clear is asserted (but Preset is not) Q goes LOW and all other inputs are irrelevant.



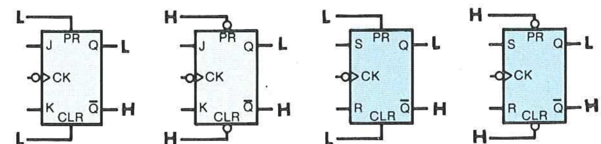
When Preset and Clear are both asserted both outputs are HIGH but will not persist even if both Preset and Clear are unasserted at the same time.



When Preset is unasserted after Clear has been unasserted Q will remain HIGH until a clock pulse arrives.



When Clear is unasserted after Preset has been unasserted Q will remain LOW until a clock pulse arrives.

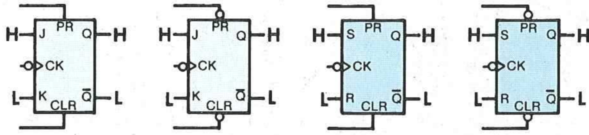


J-K and R-S Edge-triggered Flip-flops

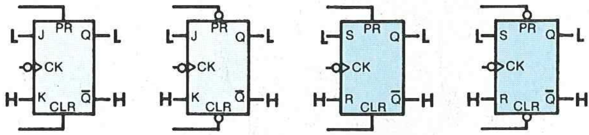
Assuming both Preset and Clear have been unasserted.

If the J-K or R-S (data) inputs are in opposite states the outputs change to correspond with the inputs when the down-going edge of a clock pulse arrives.*

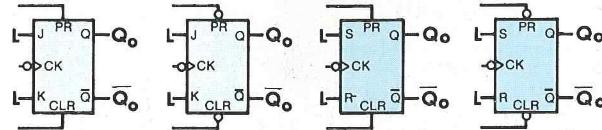
$J = Q$ and $K = \overline{Q}$ $S = Q$ and $R = \overline{Q}$



Same as above but with inputs reversed.



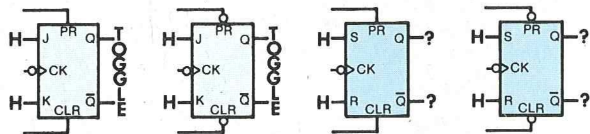
If the J-K or R-S (data) inputs are both in the LOW state the outputs do not change from the existing states when the down-going edge of a clock pulse arrives.*



If the data inputs are both HIGH when the down-going edge of a clock pulse arrives:*

The outputs of a J-K flip-flop will reverse, toggle.

The outputs of an R-S flip-flop will be indeterminate.



NOTES: Positive LOGIC: HIGH is TRUE (1) and LOW is FALSE (0).

Preset (PR) is sometimes called Set (S).

Clock (CK) is sometimes symbolized Cp.

Clear (CLR) is sometimes called Reset (R).

A function is asserted when HIGH except on input lines terminated with a small circle (-o|).

Asserted inputs are circled:

***When the up-going edge of a clock pulse transfers data to the outputs the clock input is symbolized without a small circle**

Master-slave Flip-flops

Master-slave flip-flops recognize and store the states of the data inputs during and following one edge of a clock pulse and transfer those states to the outputs during and following the next edge. The clock pulse edge that causes a transfer is symbolized on the clock input line.*

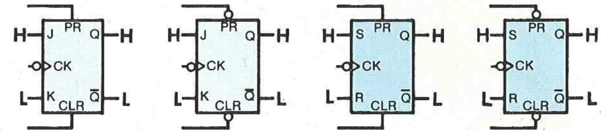
The state of a data input line should normally not change during the interval between the leading and trailing edge of a clock pulse. If the state does change during this interval a HIGH level probably will be stored and transferred. This is called "ones-catching." Master-slave flip-flops with "data-lockout" will store only the level that exists during and immediately following the leading edge transition.

J-K and R-S Pulse-triggered (Master-slave) Flip-flops

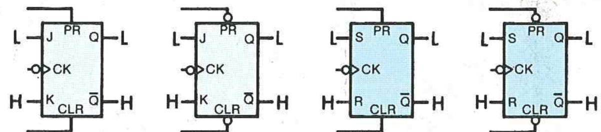
Assuming both Preset and Clear have been unasserted.

If the J-K or R-S (data) inputs were in opposite states during the arrival of the up-going edge of a clock pulse the next down-going edge will transfer those stored states to corresponding outputs.*

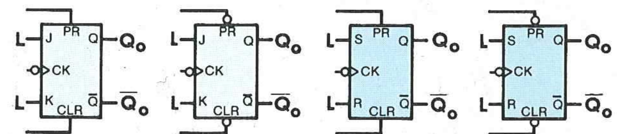
$J = Q$ and $K = \overline{Q}$ $S = Q$ and $R = \overline{Q}$



Same as above but with inputs reversed.



If the J-K or R-S (data) inputs were both in the LOW state during the arrival of the up-going edge of a clock pulse the next down-going edge will transfer no change to the outputs.*



When the down-going edge of a clock pulse arrives following an up-going edge that occurred while both data inputs were HIGH:

The output of a J-K flip-flop will reverse, toggle.

The outputs of an R-S flip-flop will be indeterminate.